# Time-Stretch Accelerated Processor for Real-time, In-service, Signal Analysis

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***Abstract*—We demonstrate real-time, in-service, digital signal analysis of 10 Gbit/s data using a 1.2 Tbit/s burst-mode digital processor. The processor comprises a time-stretch front-end and a custom data acquisition and real-time signal processing back-end. Experimental demonstration of real-time, in-service, signal integrity analysis of streaming video packets at 10 Gbit/s is presented.**

## I. INTRODUCTION

The rapidly increasing demand for higher data rates in Internet data communication demands better network performance. This in turn requires the implementation of faster ways to monitor degradations/faults in the system and to perform efficient, automated corrective actions to the affected unit in the optical fiber communication network [1]. Rapid optical performance monitoring (OPM) [2-4] provides important information about mean time to repair and mean time to failure of network elements and can be used to ensure high Quality of Transmission (QoT). Important performance metrics, such as bit error rate (BER) [4], rise-fall times, eye-opening, and jitter, can be determined from the eye-diagrams of the data signals [5]. Estimating these parameters quickly is important for active performance monitoring in high-speed networks to enable agile optical networking [4].

Real-time, in-service, signal analysis for degradation/fault detection can meet the challenge and help improve QoT of the network. It also can benefit radio frequency (RF) communication technology by enabling adaptive modulation schemes based on the estimated real-time, in-service BER [6]. Real-time, in-service, eye diagram generation and BER estimation has always been a challenging problem. Prior art utilizing a front-end analog-to-digital converter (ADC) [7] to digitize the data signal in real-time and then perform BER estimation on in-service data has considerable limitations. Performing real-time signal analysis on high-speed data (> 5 Gbit/s) requires very high bandwidth digitizers with very high resolution, which is difficult to achieve [8] and also a real-time processing platform that could handle the huge amount of data that is being generated by sampling at a rate higher than the bandwidth of the signal. High performance ADCs that support very high analog bandwidths are also very power hungry and require expensive process technologies [8, 9].

As opposed to traditional approaches, the time-stretched enhanced recording (TiSER) digitizer [9-16] enables ultra-high throughput and precision capture of wide-band analog signals by slowing them down so they can be digitized in real-time with a slower, higher-resolution, more energy efficient analog-to-digital converter. By contrast, a sampling or equivalent-time oscilloscope performs signal integrity measurements by relying on the repetitive or clock synchronous nature of the input signal for digital reconstruction. An equivalent-time oscilloscope samples signals at megahertz frequencies (up to 10 MHz) and then reconstructs the signals digitally, which requires a long time for accurate measurements. Even though it can achieve equivalent-time bandwidths of up to 110 GHz, it cannot capture single, rare and non-repetitive signal events. The real-time TiSER oscilloscope, on the other hand, features an extremely fast acquisition time and employs real-time burst sampling (RBS) modality to achieve much higher sampling throughput compared to conventional communication signal analyzers. It can also record ultra-fast, non-repetitive dynamics that occur within the burst period, which is impossible to achieve in a conventional sampling oscilloscope [10].

The time-stretch technique is at the heart of various high-throughput, real-time instruments developed for science, medicine and engineering applications. The record throughput of instruments such as serial time-encoded amplified microscopes (STEAM), MHz-frame-rate bright-field cameras, ultra-high-frame-rate fluorescent cameras for biological imaging, has enabled the characterization of “rare events” as well as the discovery of optical rogue waves and the detection of cancer cells in blood with sensitivity of one cell in a million [17, 18].

In this paper, we report a 1.2 Tbit/s real-time burst-mode digital signal processor enabled by TiSER for optical performance monitoring and RF signal integrity analysis. The processor combines the time-stretch pre-processing, analog-to-digital conversion, clock recovery from the data and digital processing on a single physical platform. The system eliminates read/write transfer bottlenecks and software processing latencies, using parallel digital signal processing (DSP). The in-service, captured time-stretched data is digitally processed in real-time, using a field programmable gate array (FPGA) with a large local random access memory (RAM)

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bank. It can also be streamed to a host PC for additional analysis.

We demonstrate real-time digitization and processing of 10 Gbit/s RF signals generated by a pseudo-random bit sequence (PRBS) generator to generate real-time eye diagrams. The recovered data, along with synchronization information, is streamed to a PC, where eye-diagrams are analyzed in software to estimate the BER. We also demonstrate, for the first time, real-time, in-service, eye diagram generation and BER estimation on 10 Gbit/s On-off keying (OOK) modulated streaming video packets sent between two nodes of a commercial optical network platform (ONP), Fujitsu Flashwave 9500.

## II. Time-Stretch Accelerated Real-time Processor

The prototype system developed and described here includes a photonic time-stretch front-end and a custom designed high-speed electronic back-end with an on-board ADC, a 10 Gbit/s clock and data recovery (CDR) module, an FPGA (Xilinx Virtex 6, XC6VLX240T), a high-speed RAM bank, and high-speed PC interfaces (Fig. 1).

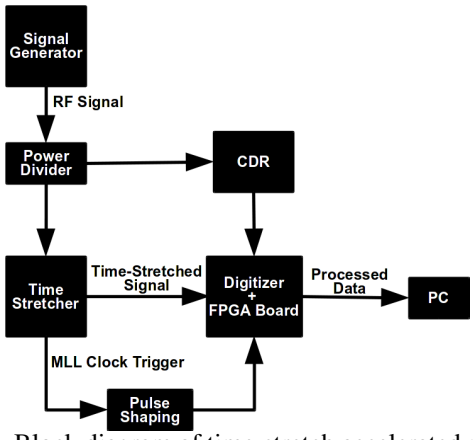



Figure 1. Block diagram of time-stretch accelerated processor

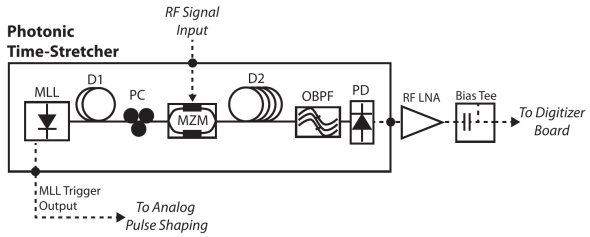



Figure 2. Schematic of the photonic time-stretch front-end [15].

The photonic time-stretch front-end (Fig. 2) consists of a femto-second mode locked laser (MLL) operating at ~ 36.7 MHz with 30 mW output power, and < 1 ps pulse width [15]. A linearly chirped optical signal, obtained by dispersing the pulses in a dispersion compensating fiber (DCF), D1, is modulated by the incoming electrical data, using a Mach-Zehnder modulator, which supports up to 40 Gbit/s. As a second step, the data signal is stretched in time by the propagation through a second dispersive fiber (D2), which reduces its analog bandwidth to fit within that of the 3 GSamples/s digitizer. The stretch factor [10] is given by,

$$\text{Stretch factor} = 1 + D2/D1 \quad (1)$$

With this approach, fast data can be captured in real-time by using a slow, high-resolution ADC. The effective temporal resolution of real-time TiSER after time-stretch, however, scales with the stretch factor, which results in an effective sampling rate of stretch factor times the sampling rate of the backend digitizer. The dispersion for D1 and D2 was chosen to have a stretch factor of 50, so that the effective sampling rate of the system is 150 GSamples/s. The output of the photo-diode (PD) is amplified, DC shifted and fed as an analog input to the electronic back-end board (Fig. 2). A small fraction of the laser signal is sent to a separate PD (not shown in Fig. 2) and used to generate a synchronization (SYNC) pulse train that is inputted to the FPGA's general-purpose I/O terminals. Pulse conditioning is necessary in order to appropriately trigger the FPGA, i.e., to comply with the FPGA input terminal logic levels. To this end, the trigger signal is filtered, inverted, amplified and shifted by a DC bias.

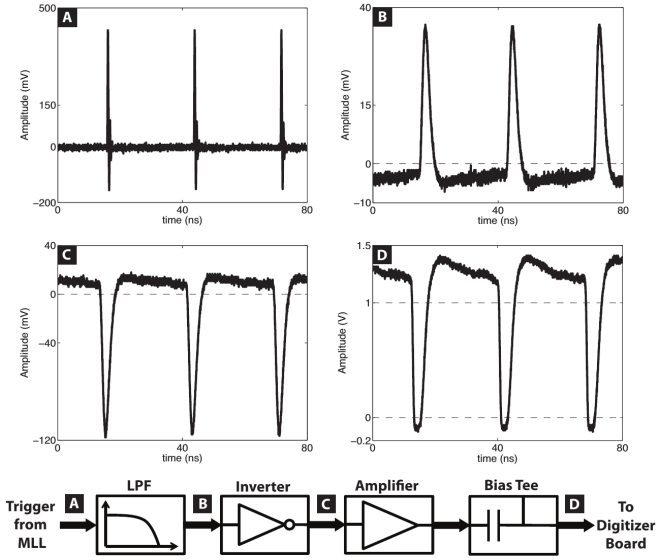



Figure 3. Analog RF electronics to reshape MLL SYNC pulse [15]

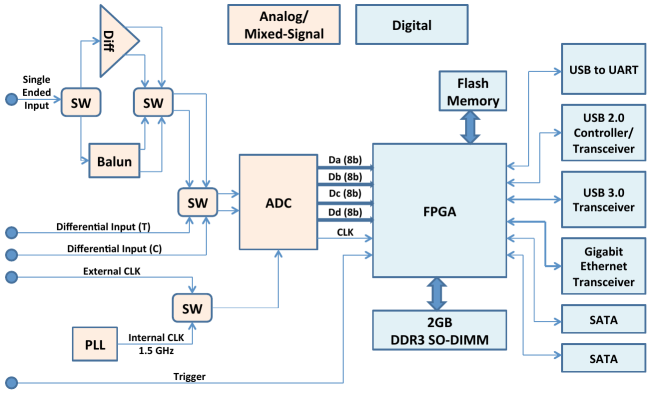



Figure 4. Block diagram of the custom designed electronic back-end digitizer system [15].

The custom digitizer board (Fig. 4) uses an 8-bit ADC (National Semiconductors ADC083000) with a maximum sampling rate of 3 GSa/s. The ADC's digitized outputs are demultiplexed to four 8-bit ports, each of which outputs four bytes of digitized sample points at double the data rate (DDR) of the 312.5 MHz differential output clock. This differential output clock is divided by two inside the FPGA, which consequently comprises the main computation clock of 156.25 MHz. The ADC and the entire FPGA system are synchronized to the data clock by using the clock recovered from the incoming data signal by the CDR module.

## III. Real-time Data Recovery on FPGA and Eye Diagram Generation

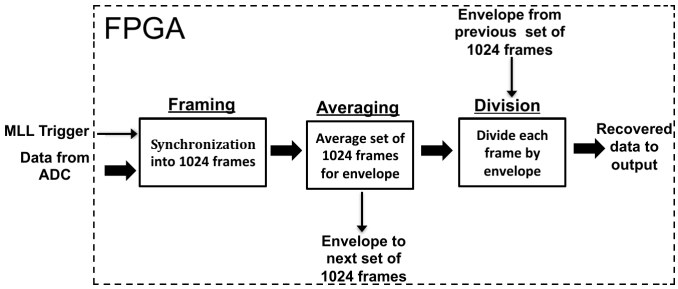



Figure 5. Block diagram of the logic implemented in FPGA

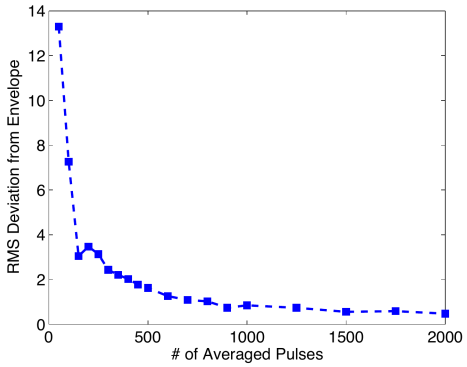



Figure 6. RMS deviation from the true envelope [15]

After time-stretching, each modulated laser pulse is of the form

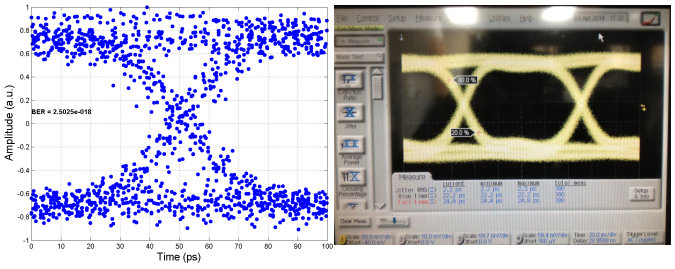
$$\text{Pulse}(t) = \text{Env}(t)\,[1 + \text{Sig}(t)], \qquad (2)$$

where Env(t) is the spectral envelope of the MLL pulse after dispersion and Sig(t) is the stretched signal of interest [11].

Digitally recovering the time-stretched data poses significant challenges, including dynamically synchronizing the FPGA to the MLL pulse, determining the envelope of the time-stretch carrier pulse, and removing the envelope from each captured modulated pulse. In order to meet these requirements, the logic design implemented on the FPGA is segmented into three modules, running in parallel and pipelining data to each other (Fig. 5). The first module continuously synchronizes the FPGA with the time-stretched pulses, and performs operations in the time domain, separating the time-stretch pulse train into single-pulse frames. Each frame is then sent to a second module, which recovers the time-stretch spectral envelope. To finally recover the original data, the third module divides the time-stretch pulses by the recovered spectral envelope.

To ensure an accurate envelope calculation, a sufficient number of pulses have to be averaged. To determine an appropriate number of frames averaged, we calculated the root mean square (RMS) deviation from the reference envelope (generated by averaging > 3000 frames) for varying numbers of frames averaged. This analysis demonstrated that the RMS deviation flattens out beyond 1000 Frames (Fig. 6). We consequently chose an averaging over 1024 pulses to compute the envelope. This obviates division operation in digital logic which reduces FPGA resource consumption. Since the laser repetition rate is ~ 27.2 ns, and real-time eye diagrams are generated for every 1024 laser pulses, the acquisition time of real-time TiSER is ~ 28 microseconds, which is significantly lower than that of equivalent-time oscilloscopes (seconds to minutes).

The data recovery is performed by dividing the synchronized frames by the computed envelope with single precision floating-point. The recovered data and the synchronization count are sent to the PC via USB 2.0 or Gbit Ethernet (GBE). Since the PRBS clock synchronizes both ADC and FPGA, the number of sample points that make up one unit interval (UI) of the PRBS can be determined. A MATLAB code uses this synchronization count to generate the eye diagrams of the recovered data (Fig. 7) and to estimate the BER.




(a) (b)

Figure 7. 10 Gb/s data Eye-diagram: (a) Real-time TiSER with a stretch factor of 50; (b) Digital Sampling Oscilloscope (shown for comparison).

For the eye diagrams shown in Fig. 7., as mentioned earlier the acquisition time for real-time TiSER is ~ 28 microseconds, while the acquisition time for the for sampling oscilloscope exceeds two minutes. This makes real-time TiSER ideally suited for feedback control in optical networks employing software defined network (SDN) controllers. The effective burst-mode sampling rate for real-time TiSER is 150 GSamples/s, which is considerably higher than real-time oscilloscopes for the same degree of resolution. The jitter present in the eye-diagrams can be attributed primarily to the one-sample point jitter of the framing module. Future logic designs can implement interpolation to reduce the one-sample point jitter upon framing, potentially improving the time-domain accuracy of the acquisition system.

## IV. Real-time In-service Optical Performance Monitoring on a Commercial Platform

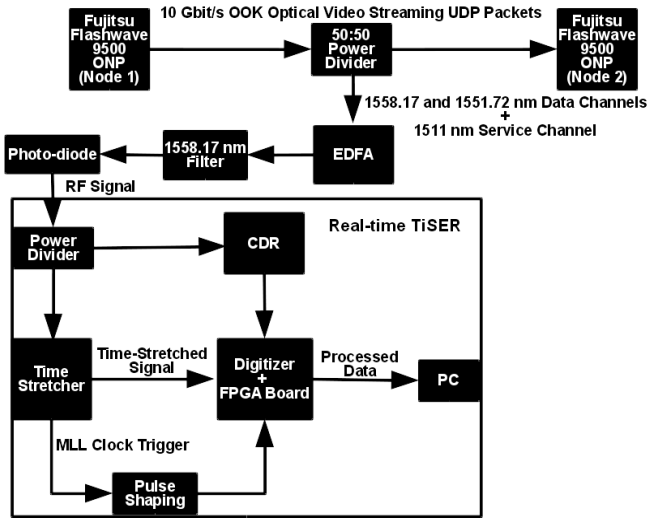
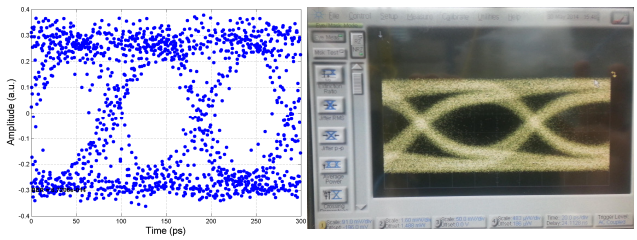



Figure 8. Setup for real-time, in-service, eye diagram generation of 10G OOK streaming video packets between two Fujitsu Flashwave 9500 nodes.

The Fujitsu Flashwave 9500 is a commercial optical networking platform that can support up to 100 Gbit/s transponder and muxponder line cards. For the real-time, in-service, optical performance measurement, two such Fujitsu Flashwave 9500 nodes each having one 10 Gbit/s OOK modulation based transponder line cards were used and from node 1, a high definition (HD) video was streamed to node 2 as User Datagram Protocol (UDP) packets. As shown in Fig. 8, the optical power going from node 1 to node 2 is tapped using a power divider and amplified by an Erbium Doped Fiber Amplifier (EDFA). There are three wavelengths present in the link that connect node 1 to node 2: the data channel at 1558.17 nm, another data channel at 1551.72 nm and a service channel at 1511 nm. The data channel wavelength, which has the video data, i.e., 1558.17 nm is filtered to remove the service channel wavelength and is then provided as input to a photodiode receiver to obtain the electrical RF signal. The output of the photo detector is power-divided and provided as an input to both the TiSER and the CDR module. This is done in order to recover the data rate clock, which subsequently undergoes frequency division to generate the ADC clock frequency, which is half of its sampling rate.




(a) (b)

Figure 9. (a) Real-time TiSER eye diagram for the 10 Gbit/s video UDP packets with a stretch factor of 50; (b) eye diagram obtained on a sampling oscilloscope (shown for comparison)

The eye diagrams obtained from both the time-stretch accelerated processor and the sampling scope are shown in Fig. 9 (a) and (b), respectively. The experimental demonstration of real-time, in-service, optical performance monitoring on 10 Gbit/s video packets on the commercial platform exhibits the capability of real-time TiSER to be used as a feedback signal to the software defined networking control plane to enable agility in the optical network to perform automated network restoration, disaster recovery, efficient routing and bandwidth management, etc.

## V. Conclusion

We have demonstrated real-time, in-service, eye-diagram generation and BER estimation of 10 Gbit/s data using a real-time 1.2 Tb/s burst-mode processing, consisting of a time-stretch front-end and a customized electronic back-end. We have also demonstrated, for the first time, real-time, in-service, optical performance monitoring using eye diagrams and BER estimation on a 10 Gbit/s OOK modulation scheme for video stream packets sent between two Fujitsu Flashwave 9500 nodes, a commercial optical network platform. The real-time TiSER implementation has an effective sampling rate of 150 GSamples/s, and a very fast acquisition time of ~ 28 microseconds. The time-stretch accelerated processor can perform BER estimation for data rates up to 40 Gbit/s, which is only limited by the bandwidth of the electro-optic modulator [10]. This technology is well suited for and aimed at real-time, in-service, digital performance monitoring for optical networks such as degradation/fault detection, correlation and localization, reliable signaling to notify other nodes, efficient routing algorithms, bandwidth management, fast network restoration schemes, and as a high bandwidth RF signal analysis tool. The proposed real-time, in-service, optical performance monitoring solution can provide necessary feedback to the SDN control plane to implement agile optical transport networks. Extension of the single channel time-stretch front-end to a parallel array can extend the current burst-mode operation to continuous-time [16].

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